# REMARKS

In the July 5, 2006 Office Action, the Examiner rejected claims 1 and 3-20 under 35 U.S.C. 102(b), as being anticipated by U.S. Patent No. 6,414,609 to Zukawa et al. (hereinafter "Zukawa"). In the present amendment, claims 1 and 16 have been amended to incorporate the existing requirements of cancelled claims 7 and 19, respectively, and claim 5 has been amended to correct a typographical error. Accordingly, Applicants submit that there are no new issues raised by Applicant's amendments, and hereby traverse the pending rejection and request that the rejected pending claims be reconsidered and allowed for the reasons set forth herein.

As variously described and claimed in each of the independent claims, Applicants have disclosed a descriptor-controlled scheme for aligning and merging packet data whereby data on a first bus having a first data width is transferred to a second memory bus having a second width. By using descriptors to control packet memory transfer operations, DMA data transfers may be routed for a plurality of channels, either as a write operation to memory from one or more packet interface circuits, or as a read operation from memory to one or more output ports.

Rather than disclosing the use of an offset specified in a descriptor to control the alignment and merger of data transfers (such as variously recited in at least independent claims 1, 9 and 16), Zukawa instead describes a data width conversion apparatus (shown in Figure 1) which is controlled by an "input write enable signal WEI representative of timing for reading the input data and a signal representative of a data width of the input data entered at that time as well as the input data." Zukawa, Figure 1, col. 7, lines 60-64. In particular, the Zukawa Patent discloses that these signals are provided to the shift amount-computing unit 18 which "computes the respective shifting amount of the first block shifter 11 and the second block shifter 12, and the barrel shifter 15 in accordance with information as to the data width of the input data sequentially inputted, and outputs a control signal indicating the respective shifting amount to the first block shifter 11 and the second block shifter 12, and the barrel shifter 15." *See*, Zukawa Patent, column 8, lines 1-8. The failure to disclose a descriptor-based data transfer scheme should come as no surprise, since Zukawa never mentions or suggests a direct memory access (DMA) data transfer scheme for transferring data directly to memory. Instead, the Zukawa Patent, which is a Fujitsu patent, is directed primarily to a data transfers over a network access server between a digital video camera and the Internet. *See*, Zukawa Patent, Figures 7-10 and related description. Accordingly, Applicants submit that all pending claims should be allowed.

Another deficiency is that Zukawa fails to meet the requirement of transferring data on a plurality of channels from a first bus to the memory bus (as variously recited in claims 1-8, 13 and 20). With regard to the "plurality of channels" requirement, the Examiner cites Zukawa's disclosure of Figure 5 and col. 11, line 66 to col. 12, line 2 ("The input selector 41 sequentially receives data from the input FIFO memory and distributes the sequentially received data to the data processing sections in accordance with the selection signal S1."). However, Zukawa's Figure 5 does not disclose a "packet manager circuit coupled between the first bus and the memory bus to transfer data from each of a plurality of channels" (as recited in claim 1), but instead depicts an embodiment where an input selector 41 and output selector 47 are used to selectively route one of a plurality of data processing sections 42-46 to a single data width conversion apparatus 10. *See*, Zukawa, col. 11, lines 54-65. In addition, the referenced disclosure nowhere suggests using a plurality of buffer regions in the packet manager's input buffer for the plurality of channels. As for the Examiner's cited passage (quoted above), Applicants respectfully submit that this passage in no way meets the variously recited "plurality of channels" requirements of claim 7 (now incorporated into claim 1), claim 8, claim 13 or claim 20. In short, Zukawa's "selector 41" does not disclose how data on a plurality of channels is transferred to a memory bus using a packet manager input buffer having buffer regions for each channel, as recited in claim 1. Because Zukawa discloses that only a single channel of data packets is routed through Zukawa's data width conversion apparatus 10 at a time, Applicants submit that at least claims 1-8, 13 and 20 should be allowed.

Zukawa also fails to meet the requirements of a "multiprocessor switching device" and of an "interface circuit for receiving packet data for a plurality of channels and transferring the packet data on the plurality of channels to a first bus having a first data width" as recited in claim 1. Applicants respectfully submit that the Examiner's analysis has improperly glossed over these requirements because none of the referenced passages from Zukawa teach or in any way suggest either of these requirements. For example, there is nothing in Figures 5 and 6 or column 12, lines 24-26 having anything to do with a multiprocessor switching device, as asserted by the Examiner. *See*, Office Action, p. 2 (July 5, 2006). Likewise, there is nothing in column 1, lines 7-10 having anything to do with the recited "first interface circuit." *Id.* Accordingly, Applicants submit that at least claims 1-8 should be allowed.

## CONCLUSION

In view of the amendments and remarks set forth herein, Applicants respectfully submits that all pending claims are in condition for allowance. Accordingly, Applicants request that the rejections be withdrawing and that a Notice of Allowance be issued. Nonetheless, should any issues remain that might be subject to resolution through a telephone interview, the Examiner is requested to telephone the undersigned at 512-338-9100.

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Respectfully submitted,

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